

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

In re Application of:
Jon M. Huppenthal, Thomas R. Seeman, Lee A. Burton

Serial No.: 09/932,330

Filed: August 17, 2001

For: **SWITCH/NETWORK ADAPTER PORT FOR
CLUSTERED COMPUTERS EMPLOYING A
CHAIN OF MULTI-ADAPTIVE
PROCESSORS IN A DUAL IN-LINE
MEMORY MODULE FORMAT**

Confirmation No. 4801

Art Unit: 2182

Examiner: Sorrell, Eron J.

Customer No. 25235

Docket No. SRC012

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF UNDER 37 C.F.R. § 41.37- AMENDED

I. Real Party in Interest

SRC Computers, Inc.
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II. Related Appeals and Interferences

No other appeals or interferences are currently known to Appellant that will directly affect, be directly affected by, or have a bearing on the decision to be rendered by the Board of Patent Appeals and Interferences in the present appeal.

III. Status of Claims

Claims 1-51 were originally filed. Claims 1-36 are pending in the application with claims 37-51 being canceled. No claims have been allowed.

Claims 1-4, 7-10, 12-16 and 19-24 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,052,134 by Foster ("Foster") in view of U.S. Patent No. 4,972,457 by O'Sullivan ("O'Sullivan").

Claims 25-28, 31-34 and 36 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Foster in view of O'Sullivan in further view of U.S. Patent No. 5,889,959 by Whittaker ("Whittaker").

Claims 29 and 30 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Foster in view of O'Sullivan as applied to claim 25, in further view of U.S. Patent No. 6,598,199 ("Tetrick").

Claim 36 was rejected under 35 U.S.C § 103(a) as being unpatentable over Foster in view of O'Sullivan and further in view of Whittaker as applied to claim 25, and further in view of U.S. Patent No. 6,581,157 by Chiles et al. ("Chiles").

Claims 1-36 stand finally rejected.

Independent claims 1, 13 and 25 are the subject of this appeal.

IV. Status of Amendments

All the claim amendments have been entered. No amendments have been filed subsequent to the Final Office Action mailed on April 20, 2006.

V. Summary of Claimed Subject Matter

Claims 1, 13, and 25 are at issue in this Appeal. The following concise explanation of the subject matter defined in each of the independent claims 1, 13, and 25 involved in this Appeal refer to the specification by page and line numbers, and to the drawing by reference characters.

The computer system 200 of claim 1 is clearly shown in Figure 5 and is described beginning at line 6 on page 15 of the specification. As shown in Figure 5, at least one processor 202 is coupled to a peripheral bus control block 206 and a memory module bus 216 via a controller 204. At least one peripheral bus slot 208 is coupled to the peripheral bus control block 206 via a peripheral bus 210. (reference page 15, lines 15-26) The memory module bus 216 is also coupled to at least one memory module slot 214. (reference page 15, lines 31-34 of the specification) A processor element 212 associated with at least one of the memory module slots 214 provides a direct data connection between an external device, coupled to the processor element 212, and the memory module slot 214 enabling the direct exchange data between the external device and the memory module bus 216. (reference page

16, lines 2-10 of the specification) Since the external device gains a data connection through the memory module slot, it can exchange data using the memory bus rather than the peripheral bus.

The significance of the subject matter of claim 1 can be realized by referring to Figure 5. Figure 5 shows a typical data rate associated with a peripheral bus 210 and the typical data transfer rate associated with the memory module bus 216. As shown, the data transfer rate associated with a memory bus is significantly greater than that of the peripheral bus.

Each aspect of claim 13 is also set forth in Figure 5. As discussed in the paragraph beginning at line 15 on page 15 (see lines 28-30) of the specification, the slots 208 may alternately comprise accelerated graphic ports or system maintenance bus connections. In the graphic case and as referring back in the same paragraph, a controller couples at least one processor 202 to a graphics control block 206 and a memory module bus 216. The graphic control block 206 is further coupled to at least one graphics connection 208 via a graphics bus 210. Again the memory module bus 216 is coupled to at least one memory module slot 214. Associated with at least one memory module slot 214 is a processor element 212. The processor element 212, which is further coupled to an external device, provides a direct data connection between the external device and the memory module bus 216 so as to enable data exchange directly between the external device and the memory module bus 216.

Claim 25 introduces the aspect that the peripheral bus control block 206 of claim 1 can be, in the alternative, a system maintenance control block as is disclosed on lines 28-30 of page 15 of the specification. The system maintenance control block 206 is coupled to a system maintenance bus connection 208 via a system maintenance bus 210. The paragraph beginning at line 3 on page 17 describes these aspects of the invention.

VI. Grounds of Rejection to be Reviewed on Appeal

A. Claims 1 and 13 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,052,134 by Foster in view of U.S. Patent No. 4,972,457 by O'Sullivan.

B. Claim 25 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Foster in view of O'Sullivan in further view of U.S. Patent No. 5,889,959 by Whittaker.

VII. Argument

Rejection of claims 1 and 13 based upon Foster in view of O'Sullivan and claim 25 based upon Foster in view of O'Sullivan and in further view of Whittaker under 35 U.S.C. §103 is Improper.

In the Final Office Action of April 20, 2006, claims 1 and 13 were rejected under 35 U.S.C. § 103(a) as being unpatentable based upon Foster in view of O'Sullivan. In the same Office Action, claim 25 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Foster in view of O'Sullivan in further view of U.S. Patent No. 5,889,959 by Whittaker. These rejections are traversed based on the following remarks. The Appellants request that the rejections be reversed as not being properly supported.

Claim 1 states:

1. A computer system comprising:
 - at least one processor;
 - a controller for coupling said at least one processor to a peripheral bus control block and a memory module bus;
 - at least one peripheral bus slot coupled to said peripheral bus control block by a peripheral bus;
 - at least one memory module slot coupled to said memory module bus; and
 - a processor element associated with said at least one memory module slot for providing a direct data connection between an external device coupled thereto and the memory module slot enabling data exchange directly between the external device and the memory module bus. (emphasis added)

Claim 13 states:

13. A computer system comprising:
 - at least one processor;
 - a controller for coupling said at least one processor to a graphics control block and a memory module bus;
 - at least one graphics bus connection coupled to said graphics control block by a graphics bus;
 - at least one memory module slot coupled to said memory module bus; and
 - a processor element associated with said at least one memory module slot for

providing a direct data connection between an external device coupled thereto and the memory module slot enabling data exchange directly between the external device and the memory module bus. (emphasis added)

Claim 25 states:

25. A computer system comprising:
- at least one processor;
 - a controller for coupling said at least one processor to a system maintenance control block and a memory module bus;
 - at least one system maintenance bus connection coupled to said system maintenance control block by a system maintenance bus;
 - at least one memory module slot coupled to said memory module bus; and
 - a processor element associated with said at least one memory module slot for providing a direct data connection between an external device coupled thereto and the memory module slot enabling data exchange directly between the external device and the memory module bus. (emphasis added)

Section 103(a) of Title 35, United States Code, directs that a patent may not be obtained if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious. This subjective inquiry is fashioned to occur at the time the invention was made by a person having ordinary skill in the art to which the subject matter pertains. To form a *prima facie* case of obviousness under 35 U.S.C. § 103(a) and in accord with section 2143 of the MPEP, three basic criteria must be met before subject matter sought to be patented may be rendered unpatentable. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify a reference or to combine reference teachings that would make the subject matter obvious. Second, there must be reasonable expectation that the combined teachings of the references cited by the examiner will succeed in creating the claimed invention. And finally, the prior art references, when combined, must teach or suggest all of the claim limitations. In this case, the Examiner has failed to meet any of these requirements, let alone all three.

The Examiner has failed to show that one skilled in the art would reasonably expect to succeed in creating the claimed invention based on the teachings of Foster and O’Sullivan. The Examiner has also failed in providing a sufficient source of motivation or suggestion for one skilled in the art to combine Foster with O’Sullivan. Finally, the Examiner overlooked a key limitation of the claimed invention and thereby has failed to show that the combination of Foster and O’Sullivan teach or suggest all of the claimed limitations. Each of these issues are discussed in turn in the text that follows.

1. Modifying Foster by the teachings of O’Sullivan fails to provide a reasonable expectation of success to produce the Appellants’ claimed subject matter because neither O’Sullivan nor Foster address and solve key communication barriers inhibiting the coupling of an external processor directly to the memory module bus.

The Appellants’ invention claims direct data exchange between an external device and the memory module bus. One of average skill in the art at the time of the Appellants’ invention would not expect the combined teachings to Foster and O’Sullivan to produce such a direct data exchange. A proper analysis under 35 U.S.C. §103(a) includes the determination of “whether the prior art would also have revealed that in so making or carrying out, those of ordinary skill would have a reasonable expectation of success.” *Noelle v. Lederman*, 355 F.3d 1343, 69 U.S.P.Q.2d 1508 (Fed. Cir. 2004). While an absolute expectation of success is not necessary, the combined art must provide a reasonable expectation that one skilled in the art will succeed in making the claimed subject matter as a whole. As explained by the Federal Circuit, at least some degree of predictability is required. *Id.* “To have a reasonable expectation of success, one must be motivated to do more than merely to vary all parameters or try each of numerous possible choices until one possibly arrived at a successful result, where the prior art gave either no indication of which parameters were critical or no direction as to which of many possible choices is likely to be successful.” *Medichem, S.A. v. Rolabo, S.L.* 437 F.3d 1157, 1165 (C.A.Fed. (N.Y.), 2006). Foster in view of O’Sullivan provides no indication, no direction, and no such reasonable expectation of success. To achieve the claimed invention through the teachings of Foster and O’Sullivan, one skilled in the art would be required to vary numerous parameters, communication protocols, and other choices to achieve the result claimed by the Appellants.

The Examiner fails to offer any evidence that one skilled in the art would reasonably expect a modification of Foster, based on the teachings of O'Sullivan, would succeed in creating the Appellants' claimed invention. Instead, the Examiner suggests in the recent Advisory Action that an expectation of success exists since the claims have no limitations addressing the communication barriers between coupling an external processor directly to a memory bus. The Examiner's statement belies his position. The prior art and surrounding circumstances must provide to one skilled in the art a reasonable expectation to succeed in creating the invention, not a reasonable reason to attempt to try to create the invention. Furthermore, it is the Examiner's burden to show a reasonable expectation of success based on the cited art, not the Appellants' burden to show an expectation of failure. By justifying his rejection on the grounds that no limitations have been added to address communication barriers, the Examiner attempts to improperly shift the burden on the Appellants by forcing them to show an expectation of failure. The Federal Circuit has clearly identified that the burden of such proof lies squarely on the Examiner and not the Applicant. *See In re Dow Chem. Co.*, 837 F.2d 469, 472 (Fed. Cir. 1988).

The Examiner has failed to meet this burden because at least one feature of the claimed invention as identified in the final limitation of claims 1, 13 and 25 is novel. One key limitation states, "a processor element associated with said at least one memory module slot for providing a direct data connection between an external device coupled thereto and the memory module slot enabling data exchange directly between the external device and the memory module bus." (emphasis added) The Examiner asserts that the combination of Foster and O'Sullivan teaches a processor associated with a memory module slot for providing a direct data connection between an external device and a memory module slot. The Examiner then asserts that the device taught by combining Foster with O'Sullivan would enable data exchange directly between the external device and the memory module bus. The Examiner's assertion is without merit. The combination of elements from Foster and O'Sullivan, as formed by the Examiner, would not enable a direct data exchange between an external device and the memory module bus. These assertions by the Examiner are completely without support and are the focus of this appeal.

As recognized by the Examiner, O'Sullivan discloses a hybrid communication control unit (a modem) that may be installed in a computer expansion slot. The hybrid communications control unit of O'Sullivan is fitted with a microprocessor to convert analog signals to digital signals and vice versa when operating apart from the computer processor. As taught by

O'Sullivan at Col 7, lines 44-46 when the unit is installed in the computer the microprocessor associated with the hybrid communication control unit can be preformed by the processor of the computer. This makes complete sense since the conversion of analog signals to digital and vice versa is a function that can be, and is more properly accomplished by the computer processor.

The processing element of the Appellants' invention allows for and manages a direct exchange of data between an external device and the memory module bus of a computer. This function cannot be accomplished by the computer's processor. Memory module slots associated with the memory module bus possess specific data transfer and latency requirements that severely limit component compatibility. O'Sullivan is silent with respect to any of these factors, as such an application of the hybrid communications control unit of O'Sullivan is beyond its scope. The Examiner asserts that the simple act of installing the hybrid communication control unit of O'Sullivan in a memory module slot would enable a direct data exchange between an external device and the memory module bus. It is this enablement, this success, that would not be reasonably expected by one skilled in the art through the teachings of Foster and O'Sullivan.

As evidence of the unreasonableness of such an expectation, the Appellants provide a true and authentic copy of an affidavit by an expert in the field of computer science and computer architecture regarding the inability of the hybrid communication control unit of O'Sullivan, if installed in a memory module slot as suggested by the Examiner, to enable direct data exchange between an external device and the memory module bus. (*see* Declaration of Evidence under 37 C.F.R. § 1.132 attached hereto.) This affidavit was submitted for entry into the record on October 11, 2006 one day prior to the filing this appeal in accordance with MPEP 716.01 (A) (3). In that submission the Appellant provided a showing of good and sufficient reason why the affidavit is necessary and not presented earlier in accordance with 37 C.F.R. § 1.116(e). As stated by one skilled in the art, it would not be reasonable to expect that a device designed as an asynchronous receiver for communication with the central bus of a computer system whose primary function is to convert analog signals to a digital format and vice versa, would enable direct data exchange between the memory module bus and an external device. To interact with the memory bus via a memory module slot the hybrid communication control device of O'Sullivan would have to emulate a memory component. The hybrid communications control unit of O'Sullivan is incapable of such an emulation.

There is no evidence to suggest that O'Sullivan even considered such an application. More importantly, one skilled in the art at the time of the Appellants' invention would recognize this considerable requirement. To accomplish such a direct exchange numerous experiments, variances in communication protocols, detailed analysis of latency issues and other factors must be considered and resolved. To all of these factors, O'Sullivan is silent.

Furthermore, and as recognized by Professor Bohm as evidenced in the attached affidavit, placing the hybrid communication control unit of O'Sullivan in the memory module slot as suggested by the Examiner would defeat the purpose of O'Sullivan. Specifically, the combination of Foster and O'Sullivan as suggested by the Examiner would destroy the object of O'Sullivan as described in Col 2, line 46 to Col. 4, line 24. A combination of art that ultimately destroys the purpose of one of the pieces of art renders that combination improper for the purpose of 35 U.S.C. § 103(a). See MPEP 2143.01 VI (stating that if the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of that reference are not sufficient to render the claims *prime facie* obvious.) See also MPEP 2143.01V (stating that if the proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification.)

One skilled in the art at the time of the Appellants' invention would recognize that the combination of Foster and O'Sullivan leaves numerous and formidable hurdles to be overcome before a direct data exchange between an external device and the memory bus as claimed could take place. These hurdles serve as further evidence supporting the antithesis of the requirement under 35 U.S.C. §103(a); that being, based on Foster in view of O'Sullivan, one skilled in the art would not reasonably expect to succeed in creating the Appellants' invention.

2. The prior art fails to provide any suggestion or motivation why one skilled in the art would modify Foster with O'Sullivan so as to render the claimed subject matter obvious.

The Examiner improperly uses the Appellants' invention as a blueprint by which to craft an unsupported rejection. The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir., 1990). According to the

Federal Circuit, this motivation may be found implicitly or explicitly: 1) in the prior art references themselves; 2) in the knowledge of those of ordinary skill in the art that certain references, or disclosures in those references, are of special interest or importance in the field; or 3) from the nature of the problem to be solved leading inventors to look to reference relating to possible solutions to that problem. See *Ruiz v. A.B. Chance Co.*, 234 F.3d 654, 57 U.S.P.Q.2d 1161 (Fed. Cir. (Mo.), 2000). To prevent the use of hindsight based on the Appellants' invention to defeat the patentability of the Appellants' invention, the Examiner must show a motivation to combine the references that create the case of obviousness. "In other words, the examiner must show reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed." *In re Rouffet*, 149 F.3d 1350, 47 U.S.P.Q.2d 1453 (Fed. Cir., 1998). The question is not whether given the Appellants' invention, could one skilled in the art craft the claimed invention using the teachings of Foster and O'Sullivan. Rather the question is would one faced with the challenge of enabling direct data exchanges between an external device and a memory module bus of a computer turn to Foster and O'Sullivan.

The Examiner asserts that it would be obvious for one of ordinary skill in the art at the time of the Appellants' invention to modify the system of Foster with the teachings of O'Sullivan. The Examiner attempts to support his assertion by stating that one skilled in the art would have been motivated to make such modifications in order to add an adapter using an existing available slot without making any hardware changes in the computer or purchasing additional equipment as suggested by O'Sullivan, however words to this effect are found nowhere in O'Sullivan. The Appellants therefore assume, as no direct statement is evident, that the Examiner is relying on the high level of skill in the art at the time of the Appellants' invention. To that extent the Examiner states, "Computers with modem cards or network interface cards are ubiquitous and it would be obvious to one of ordinary skill in the art to add one to a system in order to connect to the internet." USPTO Advisory Action of July 5, 2006. Lacking in the Examiner's assessment and in the art cited by the Examiner is the motivation to provide a direct exchange of data between an external device and the memory module bus. It is this direct exchange of data that is the essence of the Appellants' invention and is this direct exchange of data on which the focus of the inquiry with respect to motivation and suggestion

under §103(a) should be based. Simply put, the question with respect to motivation and suggestion is whether within Foster and/or O’Sullivan there is motivation to combine elements of the invention as claimed by the Appellants to enable a direct data exchange between an external device and the memory module bus. To that inquiry the answer is no.

The Court in *Rouffet* stated that to “prevent the use of hindsight based on the invention to defeat patentability of the invention, this court requires the examiner to show a motivation to combine the references that create the case of obviousness.” *Rouffet* at 1350. As in the present invention, the examiner in *Rouffet* relied on the high level of skill in the art to provide the necessary motivation. Finding such motivation absent, the *Rouffet* Court stated that “if such rote invocation could suffice to supply a motivation to combine, the more sophisticated scientific fields would rarely, if ever, experience a patentable technical advance.” *Id.* The Examiner has improperly invoked such a rote source of motivation and used the Appellants’ invention as a blueprint by which to craft his rejection.

The Federal Circuit has repeatedly warned against the use of the Appellants’ invention as a blueprint by which to build a case of obviousness. The Examiner offers no explanation of the specific understanding or principle within the knowledge of one skilled in the art that would motivate one with no knowledge of the Appellants’ invention to combine the teachings of Foster and O’Sullivan to create the Appellants’ invention. The cost savings and decreased hardware modifications cited by the Examiner as a reason to combine Foster and O’Sullivan are applicable to any invention and provide no reason why one would be motivated to turn to Foster and O’Sullivan to enable direct data exchange between external devices and the memory module bus. Put simply, the Examiner offers no foundation for modifying a memory system that dynamically enables/disables memory paging depending on the page hit to pre-charge ratio for access to the memory, as disclosed by Foster, with the teaching for a hybrid communications control unit (a modem), as taught by O’Sullivan, to form system that enables direct data exchange between an external device and the memory module bus of a computer.

The proposed modification of Foster by O’Sullivan, on which the Examiner relies in crafting his rejection, alters the principal of operation of O’Sullivan. O’Sullivan describes “a novel and improved hybrid communication system incorporating an integrated, portable unit which incuse a personal computer, cellular transmitter, modem and speakerphone, and which as

external connections for a headset, cellular control unit and land telephone line, such that any of these devices may be used with any other device. ... This is all accomplished with a control system mounted on a circuit card which fits in a modem slot or similar card receiving slot in a portable computer.” O’Sullivan Col. 2, lines 46-62. O’Sullivan then goes on to describe 6 modes of operation. In each of the various modes of operations the microprocessor manages the mode of communication between a portable computer and either a cellular telephone network or a public switched telephone network. The microprocessor transmits data from the computer to devices such as a modem for digital to analog conversion or a transceiver to initiate a cellular telephone call.

The suggested combination of Foster in view of O’Sullivan would require substantial reconstruction and redesign of the elements shown in O’Sullivan as well as change the basic principle under which the O’Sullivan construction was designed to operate. Such modifications cannot support a *prima facie* case of obviousness. *See In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959). Furthermore, the Appellants’ reiterate that based on the analysis of Professor Bohm, the combination of Foster and O’Sullivan as cited by the Examiner would render O’Sullivan unsatisfactory for its intended purpose. As stated in section 2143.01 V, “if proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification.” The *prima facie* case of obviousness must fail.

3. Foster and O’Sullivan fail to teach or suggest each and every element of the claimed invention, namely a processor element associated with at least one memory module slot for providing a direct data connection between an external device coupled and the memory module slot enabling data exchange directly between the external device and the memory module bus.

The Appellants further reiterate, and incorporate by reference, their argument that O’Sullivan does not disclose a processing element enabling the direct exchange of data between an external device and a memory module bus. The Examiner asserts that “Figure 4 [of O’Sullivan] shows communication from external devices passing through the microprocessor to the interface then on to the computer.” However, O’Sullivan remarks in Column 8, beginning at line 24, that “The computer interface 78 is preferably of the type that converses directly with a

central logic bus of the portable computer 90....” The Appellants’ invention connects an external device directly to the memory module bus so as to enable the exchange of data directly between the external device and the memory module bus.

Assuming for argument’s sake that O’Sullivan suggests connecting an external device to a memory expansion slot, the combination of Foster and O’Sullivan nonetheless fails to teach that the connection enables data from the external device to be exchanged directly to the memory bus. As previously discussed, the interface that O’Sullivan describes is ideally an asynchronous receiver that communicates to the central logic bus. While O’Sullivan does not further define a central logic bus, O’Sullivan describes communications between a hybrid communications control unit and the computer consistent with that conducted on a peripheral communication interface (PCI) bus and not directly with the memory bus.

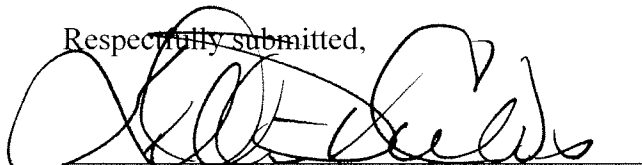
Conclusion

In view of all of the above, independent claims 1, 13 and 25 are believed to be allowable and the case in condition for allowance. Moreover, claims 2-12, 14-24 and 26-36, which depend from claims 1, 13 and 25 respectively, are also deemed allowable. Appellants respectfully request that the Examiner’s rejections based on 35 U.S.C. 103(a) be reversed for all pending claims.

Date:

09 February 2007

Respectfully submitted,



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VIII. APPENDIX OF CLAIMS ON APPEAL

1. A computer system comprising:
 - at least one processor;
 - a controller for coupling said at least one processor to a peripheral bus control block and a memory module bus;
 - at least one peripheral bus slot coupled to said peripheral bus control block by a peripheral bus;
 - at least one memory module slot coupled to said memory module bus; and
 - a processor element associated with said at least one memory module slot for providing a direct data connection between an external device coupled thereto and the memory module slot enabling data exchange directly between the external device and the memory module bus.
2. The computer system of claim 1 further comprising:
 - a control connection to said processor element coupled to said peripheral bus for indicating to said at least one processor an arrival of data on said direct data connection to said processor element and memory module bus.
3. The computer system of claim 1 wherein said memory module bus comprises a DIMM bus.
4. The computer system of claim 3 wherein said processor element comprises a DIMM physical format for retention within said at least one memory module slot.
5. The computer system of claim 1 wherein said memory module bus comprises a in-line memory module serial interface bus.
6. The computer system of claim 5 wherein said processor element comprises a in-line memory module serial interface physical format for retention within said at least one memory module slot.
7. The computer system of claim 1 wherein said external device comprises one of another computer system, switch or network.

8. The computer system of claim 1 wherein said peripheral bus comprises a PCI bus.
9. The computer system of claim 1 wherein said processor element is operative to alter data received from said controller on said memory module bus prior to transmission on said data connection to said external device.
10. The computer system of claim 1 wherein said processor element is operative to alter data received on said data connection from said external device prior to transmission to said controller on said memory module bus.
11. The computer system of claim 1 wherein said processor element comprises:
 - a field programmable gate array configurable to perform an identified algorithm on an operand provided thereto on said memory module bus and said data connection.
12. The computer system of claim 1 wherein said at least one processor comprises a plurality of processors.
13. A computer system comprising:
 - at least one processor;
 - a controller for coupling said at least one processor to a graphics control block and a memory module bus;
 - at least one graphics bus connection coupled to said graphics control block by a graphics bus;
 - at least one memory module slot coupled to said memory module bus; and
 - a processor element associated with said at least one memory module slot for providing a direct data connection between an external device coupled thereto and the memory module slot enabling data exchange directly between the external device and the memory module bus.
14. The computer system of claim 13 further comprising:
 - a control connection to said processor element coupled to said graphics bus for indicating to said at least one processor an arrival of data on said direct data connection to said processor element and memory module bus.

15. The computer system of claim 13 wherein said memory module bus comprises a DIMM bus.
16. The computer system of claim 15 wherein said processor element comprises a DIMM physical format for retention within said at least one memory module slot.
17. The computer system of claim 13 wherein said memory module bus comprises a in-line memory module serial interface bus.
18. The computer system of claim 17 wherein said processor element comprises a in-line memory module serial interface physical format for retention within said at least one memory module slot.
19. The computer system of claim 13 wherein said external device comprises one of another computer system, switch or network.
20. The computer system of claim 13 wherein said graphics bus comprises an AGP bus.
21. The computer system of claim 13 wherein said processor element is operative to alter data received from said controller on said memory module bus prior to transmission on said data connection to said external device.
22. The computer system of claim 13 wherein said processor element is operative to alter data received on said data connection from said external device prior to transmission to said controller on said memory module bus.
23. The computer system of claim 13 wherein said processor element comprises:
a field programmable gate array configurable to perform an identified algorithm on an operand provided thereto on said memory module bus and said data connection.
24. The computer system of claim 13 wherein said at least one processor comprises a plurality of processors.

25. A computer system comprising:
at least one processor;
a controller for coupling said at least one processor to a system maintenance control block and a memory module bus;
at least one system maintenance bus connection coupled to said system maintenance control block by a system maintenance bus;
at least one memory module slot coupled to said memory module bus; and
a processor element associated with said at least one memory module slot for providing a direct data connection between an external device coupled thereto and the memory module slot enabling data exchange directly between the external device and the memory module bus..
26. The computer system of claim 25 further comprising:
a control connection to said processor element coupled to said system maintenance bus for indicating to said at least one processor an arrival of data on said direct data connection to said processor element and memory module bus.
27. The computer system of claim 25 wherein said memory module bus comprises a DIMM bus.
28. The computer system of claim 27 wherein said processor element comprises a DIMM physical format for retention within said at least one memory module slot.
29. The computer system of claim 25 wherein said memory module bus comprises a in-line memory module serial interface bus.
30. The computer system of claim 29 wherein said processor element comprises a in-line memory module serial interface physical format for retention within said at least one memory module slot.
31. The computer system of claim 25 wherein said external device comprises one of another computer system, switch or network.
32. The computer system of claim 25 wherein said system maintenance bus comprises an SM bus.

33. The computer system of claim 25 wherein said processor element is operative to alter data received from said controller on said memory module bus prior to transmission on said data connection to said external device.

34. The computer system of claim 25 wherein said processor element is operative to alter data received on said data connection from said external device prior to transmission to said controller on said memory module bus.

35. The computer system of claim 25 wherein said processor element comprises:
a field programmable gate array configurable to perform an identified algorithm on an operand provided thereto on said memory module bus and said data connection.

36. The computer system of claim 25 wherein said at least one processor comprises a plurality of processors.

IX. APPENDIX OF EVIDENCE

DECLARATION OF EVIDENCE UNDER 37 C.F.R. § 1.132 (copy attached)

This affidavit was submitted for entry into the record on October 11, 2006 one day prior to the first filing of this appeal in accordance with MPEP 716.01 (A) (3). A review of the image wrapper via Private Pair indicated that the aforementioned declaration was received and entered into the image wrapper on October 11, 2006, one day prior to the receipt of the appeal brief on October 12, 2006. Subsequent communications with Examiner Sorrell on February 6, 2007 confirm that the aforementioned declaration was officially entered into the record for substantive consideration.

X. APPENDIX OF RELATED APPEALS AND INTERFERENCES

There are no copies of decisions rendered by a court or the Board to provide with this Appeal as there are no related proceedings.